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14EVE22

Second Semester M.Tech. Degree Examination, June/July 2015

Low Power VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Derive the power dissipation equation in digital CMOS circuit. **(10 Marks)**

b. Explain the two major sources of leakage current in CMOS device. **(06 Marks)**

c. A 32 bit off-chip bus operating at 5 V and 66 MHz clock rate is driving a capacitance of 25 pF/bit. Each bit is estimated to have a toggling probability of 0.25 at each clock cycle. What is the power dissipation in operating the bus? **(04 Marks)**

2 a. Explain basic principles of low power VLSI design. **(06 Marks)**

b. Draw the energy band diagram of MIS diode. What are the factors on which the threshold voltage V_T depends on? **(08 Marks)**

c. Explain the impact of technology scaling and innovation trends for low power devices. **(06 Marks)**

3 a. List the advantages and limitation of SPICE power analysis. **(06 Marks)**

b. Explain the event-driven gate level power simulation technique. **(07 Marks)**

c. Drive the expression for number of samples 'N' required for stopping criteria in Monte-Carlo simulation. **(07 Marks)**

4 a. Explain the propagation of statistical quantities in probabilistic power analysis with an example. **(08 Marks)**

b. Define signal entropy. Explain the power estimation of combinational logic using signal entropy. **(08 Marks)**

c. Find the output static probability of y = a + bc by using Shannon's decomposition method. **(04 Marks)**

5 a. Explain bus invert encoding with an example. **(08 Marks)**

b. Explain gate reorganization using basic transformation operators. **(08 Marks)**

c. Explain the architecture of bus invert encoding. **(04 Marks)**

6 a. What is pre-computation? Explain the concept of pre-charging in an inverter and comment on its power dissipation. **(10 Marks)**

b. With a neat diagram, explain the working of a 8-bit Wallace multiplier. What are its advantages? **(10 Marks)**

7 a. Explain the chip and package co-design of clock network with relevant block diagram. **(10 Marks)**

b. What are the CAD tools available at different abstraction levels? Explain with a design flow diagram for power optimization. **(10 Marks)**

8 Write short notes on:

a. Need for low power VLSI design

b. Zero skew versus tolerable skew

c. Low power SRAM

d. Signal gating **(20 Marks)**

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